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STACKED VIA STRUCTURE THAT INCLUDES A SKIP VIA

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STACKED VIA STRUCTURE THAT INCLUDES A SKIP VIA

Technical Field

Various embodiments of the present invention relate to a substrate for electronic devices that include a stacked via structure.

Background

Signals may be transmitted between layers in a substrate using vias. The vias may be stacked one on top of another depending on the design of the substrate.

Stacked vias tend to crack or delaminate at the interfaces between the vias when the vias are subjected to stress. When a via cracks or delaminates, the electronic assemblies that include such substrates may fail.

Cracking in a stacked via may also increase the resistance of the current path formed by the stacked via. The increased resistance of the stacked via may generate unwanted heat within the stacked via during operation of the substrate.

Stacked vias may be used in substrates that include a relatively high number of dielectric layers. As the number of via-to-via interfaces in a stack increases, the risk that one of the vias will crack and/or delaminate may also increase.

One technique that may be used to minimize stress throughout a stack of vias is to utilize dielectric materials in the layers of the substrate that have a lower coefficient of thermal expansion (CTE). However, the stress within the stacked via structure may not be completely eliminated when lower CTE materials are used to form the dielectric layers in a substrate.

There is a need for a substrate that includes stacked vias which are able to reliably communicate signals between dielectric layers in the substrate. The number of via-to-via interfaces within the stack of vias should be minimized to decrease cracking and/or delamination that may occur within the stacked via.

Brief Description of the Drawings

A more complete understanding may be derived by referring to the detailed description and associated figures. It should be noted that like reference numbers refer to similar items throughout the figures.

FIG. 1 is a section view illustrating a portion of a substrate that includes stacked vias.

FIG. 2 is a section view illustrating a portion of another substrate that includes stacked vias.

FIG. 3 is a section view illustrating a portion of the substrate shown in FIG. 2 with an additional via added to the stacked vias.

FIGS. 4A-4H are section views that illustrate a method of forming the substrate shown in FIG. 1.

FIG. 5 is a block diagram of an electronic system incorporating at least one substrate similar to the substrates shown in FIGS. 1-3.

Detailed Description

FIG. 1 illustrates a substrate 10 that may include vias 21A, 21B for communicating signals throughout the substrate 10, in accordance with various embodiments of the invention. Substrate 10 may include a plurality of dielectric layers 22A, 22B, 22C that are formed on a core 20. One of the vias 21A, 21B may be a first skip via 21A that extends through at least two of the dielectric layers 22A, 22B. Another via 21B may extend through at least one other of the dielectric layers 22C such that the second via 21B and the first skip via 21A are stacked on top of one another.

As used herein, vias that are stacked refers to vias that at least partially overlap. The sample embodiment illustrated in FIG. 1 shows that the longitudinal axis 23 of each via 21A, 21B may be substantially aligned with the longitudinal axis of the other vias.

FIG. 2 illustrates another sample embodiment of substrate 10. In the example embodiment illustrated in FIG.2, the second via 21B may be a second skip via 21B that extends through at least two dielectric layers 22C, 22D.

FIG. 3 illustrates another sample embodiment of substrate 10. In the example embodiment illustrated in FIG. 3, substrate 10 may include a third via 21C that extends through at least one other of the dielectric layers 22E, 22F such that the third via 21C may be stacked onto the first skip via 21A and the second skip via 21B. As shown in FIG. 3, third via 21C may be a skip via 21C that extends through at least two dielectric layers 22E, 22F.

Depending on the design of the substrate 10, any number of vias may be included in the stack of vias as long as at least one of the vias is a skip via. In addition, the skip via may be located anywhere within the stack of vias (e.g., top, bottom, or somewhere in the middle). The stack of vias may also include more than one skip via. It should be noted that a skip via may extend through two or more dielectric layers.

Utilizing one or more skip vias in a stack of vias reduces the number of via-to-via interfaces within the stack of vias. The via-to-via interfaces within a stack of vias are the sections within the stack of vias that tend to crack or delaminate when the vias are subjected to stress. Therefore, reducing the number of via-to-via interfaces within the stack of vias may make electronic assemblies that include such substrates less likely to fail.

FIGS. 1, 2 and 4A-4H illustrate a method in accordance with various embodiments of the invention. As shown in FIG. 1, the method may include forming a first via 21A and stacking a second via 21B onto the first via 21A. Although first via 21A is shown as skip via 21A, either the first via 21A or the second via 21B may be a skip via.

FIG. 2 illustrates that stacking a second via 21B onto the first via 21A may include stacking a second skip via 21B onto the first skip via 21A. In addition, stacking the second via 21B onto the first via 21A may include substantially aligning a longitudinal axis 23 of the first via 21A with a longitudinal axis 23 of the second via 21B.

FIGS. 4A-4G illustrate that forming a first via 21A in a substrate 10 may include forming a first conductive layer 24A onto a core 20 and forming a first dielectric layer 22A such that the first conductive layer 24A is between the first dielectric layer 22A and the core 20 (FIG. 4A). In various embodiments, forming a first conductive layer 24A may include plating the first conductive layer 24A onto the first dielectric layer 22A and patterning the first conductive layer 24A to form traces on the core 20.

Forming a first via 21A may further include forming a second conductive layer 24B onto the first dielectric layer 22A (FIG. 4B). The method may further include forming a second dielectric layer 22B such that the second conductive layer 24B is between the first dielectric layer 22A and the second dielectric layer 22B (FIG. 4C). In various embodiments, forming a second conductive layer

24B may include plating the second conductive layer 24B onto the first dielectric layer 22A and patterning the second conductive layer 24B to form traces on the first dielectric layer 22A.

Forming a first via 21A may further include forming an opening 25 in the first and second dielectric layers 22A, 22B (FIG. 4D). The method may further include forming a first skip via 21A in the opening 25 (FIG. 4E).

In addition, forming a first skip via 21A in the opening 25 may include filling the opening 25 with a conductive material, such as by forming a third conductive layer 24C onto the second dielectric layer 22B (FIG. 4E). In various embodiments, forming a third conductive layer 24C may include plating the third conductive layer 24C onto the second dielectric layer 22B. The method may further include patterning the third conductive layer 24C to form traces on the second dielectric layer 22B.

Forming the opening 25 in the first and second dielectric layers 22A, 22B may include drilling an opening 25 in the first and second dielectric layers 22A, 22B, such as by laser drilling. In alternative embodiments, forming the opening 25 in the first and second dielectric layers 22A, 22B may include etching the opening 25 in the first and second dielectric layers 22A, 22B.

In the example embodiment shown in FIG. 4F, the first via 21A is a first skip via 21A such that stacking the second via 21B onto the first skip via 21A may include forming a third dielectric layer 22C on the third conductive layer 24C. The method may further include forming a second opening 26 in the third dielectric layer 22C (FIG. 4G), and forming the second via 21B in the opening 26 (FIGS. 1 and 4H).

In various embodiments, forming the second via 21B in the opening 26 may include filling the opening 26 with a conductive material. The opening 26 may be filled by forming a fourth conductive layer 24D onto the third dielectric layer 22C, and then patterning the fourth conductive layer 24D to form traces on the third dielectric layer 22C.

The example methods described herein may be suitable for reducing the number of steps associated with fabricating substrates that have stacked vias. The number of steps associated with fabricating such substrates is reduced because forming one or more skip vias in a stack of vias decreases the number of drilling operations that need to be carried out in order to form the stack of vias.

The vias may be cylindrical or any other shape that facilitates fabricating substrate 10. In some embodiments, each of the vias is cylindrical with a diameter between 49um and 85um. The skip vias that extend through two dielectric layers may have a length between 58um and 92um, while the other regular vias may have a length between 24um and 36um.

Various conductive materials may be used for vias 21A, 21B, 21C and/or the conductive layers. These materials may include gold, copper, aluminum and combinations thereof.

In some embodiments, each of the conductive layers is applied to the respective dielectric layers such that the conductive layers have a thickness between 10um and 75um. The conductive layers may be applied at the same thickness, different thicknesses, or any combination thereof.

Various materials may be used for dielectric layers 22A-22F. In various embodiments, these materials may include film and liquid type insulation materials that are made of resin plus filler. The CTE value of the dielectric layers 22A-22F is typically controlled by filler content and the type of resin.

In some example embodiments, each of the dielectric layers 22A-22F has a thickness between 34um and 111um. The dielectric layers that form the substrate 10 may have the same thickness, different thicknesses, or any combination thereof.

Various materials may be used for core 20. In various embodiments, these materials may include one or more different types of resins. In some embodiments, the resins that form the core 20 may further include glass fiber cloth with one or more fillers.

The core 20 may have any thickness. In some example embodiments, the core 20 has a thickness between 650um and 850um.

FIG. 5 is a block diagram of an electronic system 40 incorporating at least one electronic assembly 30. The electronic assembly 30 may include any of the example substrates 10 described above. Electronic system 40 may be a computer system that includes a system bus 42 to electrically couple the various components of electronic system 40 together. System bus 42 may be a single bus or any combination of busses.

Electronic assembly 30 is electrically coupled to system bus 42 and may include any circuit, or combination of circuits. In one embodiment, electronic

assembly 30 includes a processor 46 that is coupled to substrate 10. As used herein, processor means any type of circuit, such as, but not limited to, a microprocessor, a microcontroller, a graphics processor or a digital signal processor. Other types of circuits that can be coupled to substrate 10 in electronic assembly 30 are a custom circuit or an application-specific integrated circuit, such as communications circuit 47 for use in wireless devices such as cellular telephones, pagers, portable computers, two-way radios, and similar electronic systems.

The electronic system 40 may also include an external memory 50 that in turn may include one or more memory elements suitable to the particular application, such as a main memory 52 in the form of random access memory (RAM), one or more hard drives 54, and/or one or more drives that handle removable media 56, such as diskettes, compact disks (CDs) and digital video disks (DVDs).

The electronic system 40 may also include a display device 58, a speaker 59, and a controller 60, such as a keyboard, mouse, trackball, game controller, microphone, voice-recognition device, or any other device that inputs information into the electronic system 40.

As shown herein, substrate 10 can be implemented in a number of different embodiments, including an electronic package, an electronic system and a computer system. The elements, materials, geometries and dimensions can all be varied to suit particular requirements.

FIGS. 1-5 are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated while others may be minimized.

Many other embodiments will be apparent to those of skill in the art from the above description. Modifications, equivalents and variations are within the scope of the appended claims.